Worksheet 1: Computer architecture

**Task 1**

1. Match up the terms on the left with the statements on the right

|  |  |  |
| --- | --- | --- |
| Accumulator |  | Points to the next instruction that needs to be executed. It is located in the Control Unit |
| Memory Address Register (MAR) |  | Used for holding the address of the  current instruction to be executed,  and the address of data to be used in instruction |
| Memory Data Register (MDR) |  | Used for holding the actual instruction or data  that is stored in RAM |
| Program Counter |  | Used for temporarily storing arithmetic  and logic results. |

2. von Neumann architecture uses the ‘stored program’ concept. Describe what this means.

3. How does the computer know whether an address contains an instruction to be executed, or data to be used in an instruction?

The computer doesn’t know wether an address contains data or an instruction. It can only tell once it has been executed

**Task 2**

4. The segment of memory shown below stores both program instructions and data.

|  |  |
| --- | --- |
| **Address** | **Data / Instruction** |
| 01 | LDA #11 |
| 02 | SUB 05 |
| 03 | STO 06 |
| 04 |  |
| 05 | 3 |
| 06 |  |

1. What is this architecture known as?

Von Neumann architechture

1. With reference to the four CPU registers below, describe how they are used to complete the program instructions stored in location1. LDA #11 means “Load the value 11”, SUB 05 means “subtract the value in location 5”. STO 06 means “store the result in location 6”. Note the use of ‘#’ to denote an actual value rather than the value in a memory location.

**Program Counter (PC)**

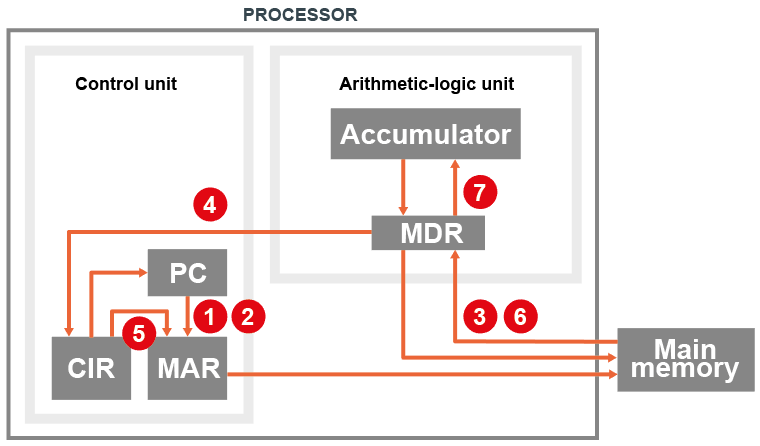
**Memory Address Register (MAR)**

**Memory Data Register (MDR)**

**Accumulator**

The program counter stores the addresses of instructions temporarily until they are processed and executed.

The memory address register stores the address of the current instruction, and then the data it uses, so it can be fetched from memory



(c) Complete the following series of steps:

The PC holds the address 02 containing instruction SUB 05.

Steps carried out in the Fetch-Execute cycle are labelled in sequence 1-7.

At step 1: the address 02 is copied to the MAR.

At step 2: the PC is incremented so it now holds 03

At step 3: the instruction at address 02 is copied to the MDR

At step 4: Instruction is copied to Current Instruction Register (CIR)

At step 5:

At step 6:

At step 7: